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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,752	04/03/2001	Makoto Nonaka	Q63936	9106

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EXAMINER
ECKERT II, GEORGE C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/823,752	Applicant(s) Nonaka
	Examiner George C. Eckert II	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 19, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above, claim(s) *17-21* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-8, 15, and 16* is/are rejected.

7) ☒ Claim(s) *9-14* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Apr 3, 2001* is/are a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *4 & 7*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Claims 17-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in Paper No. 8.

Drawings

2. The drawings are objected to because figure 2B, which is to be an enlarged view of box A from figure 2A, labels two lines as 16b and two other lines as 17b whereas the view in box A shows four lines, labeled 16a, 16b, 17a and 17b. In other words, lines 16a and 17a, though shown in box A, are not shown in figure 2B.

The drawings are further objected to for failing to show wires 26a and 27a in figure 6 as mentioned on page 16, lines 1-5. Rather, figure 6 shows wires 16 and 17 which seem to be remnants from the first embodiment. Also, figure 6 does not show wires 26a and 27a configured as combs to have the same structure as that of 26b and 27b (see page 16, lines 11-15).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 U.S.C. § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4-7, 15 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With regard to claims 4-7, claim 4 cites a bypass capacitor which lacks antecedent basis because the bypass capacitor was only earlier defined as one element of a Markush group in claim 2. Claim 7 similarly lists "said input/output device" which was only listed as a Markush element. With regard to claims 15 and 16, both claims include the limitations "said first metal wiring layers" and "said second metal wiring layers" (claim 15, lines 23-24, claim 16, lines 23 and 25) which both lack antecedent basis.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4-6 (as best understood) and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,949,098 to Mori. Mori teaches, with reference to figures 3 and 4, a semiconductor device having a plurality of wiring layers in a multilayered structure including:

an inner area 421/422 at a surface and a pad area (generally the area including pads 433) surrounding the inner area therein,

the semiconductor device comprising a device fabricated below the pad area (see figure 3).

With regard to claim 2, Mori teaches that the device is a bypass capacitor (col. 5, lines 21-29). With regard to claim 4, Mori teaches that the bypass capacitor is formed of metal layers 310, 330 and 350. With regard to claim 5, Mori teaches that the first and second wires of the metal wire layers are connected to a voltage source and ground respectively (col. 4, lines 39-53). With regard to claim 6, Mori teaches that each of the wire layers is comprised of a comb shaped wire such that teeth of the first and second wires are located between each other in the same plane (see figure 3, layer 330 where the first and second wires each comprise comb-like teeth which are located between each other).

With regard to claim 8, Mori teaches a semiconductor device including:

an inner area 421/422 at a surface, an input/output area surrounding the inner area (generally that area in which lines 441 and 442 are located), and a pad area (generally that area in which pads 432 are located) surrounding the input/output area;

the device including a plurality of input/output terminals 441/442 in the input/output area, and a plurality of pads 431/432 in the pad area;

the device including a first source voltage wire (e.g. 310) connected to a source voltage Vdd and surrounding the inner area in the pad area and a first ground wire (e.g. 350) being grounded and surrounding the first source voltage wire in the pad area;

each of the pads 431/432 being connected to the first source voltage wire and the first ground wire respectively;

the first source voltage wire being comprised of a plurality of first metal wiring layers in a multilayered structure, the first metal wiring layers being electrically connected to one another through via holes (e.g. 341) formed through first interlayer insulating films 340 sandwiched between first metal wiring layers,

the first ground wire being comprised of a plurality of second metal wiring layers in a multi-layered structure, the second metal wiring layers being electrically connected to one another through via holes 342 formed through the first interlayer insulating film 340,

each of the first and second metal wiring layers being formed in the same layer 330,

vertically adjacent first and second metal wiring layers with one of the first interlayer insulating films being sandwiched therebetween, among the first and second metal wiring layers, defining a bypass capacitor.

5. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 4-5-55380 to Sudo. Sudo teaches, with reference to figures 1a and b, a semiconductor device having a plurality of wiring layers in a multilayered structure including:

an inner area 11 at a surface and a pad area 1 surrounding the inner area therein,

the semiconductor device comprising a device fabricated below the pad area (see fig. 1b).

With regard to claim 2, Sudo teaches that the device is a bypass capacitor (see *Constitution*). With regard to claim 3, Sudo teaches that the device further comprises an input/output device below the bypass capacitor (see figure 1b). With regard to claim 4, Sudo teaches that the bypass capacitor is formed of metal layers 9 and 11. With regard to claim 5, Sudo teaches that the first and second wires of the metal wire layers are connected to a voltage source and ground respectively (see *Constitution,* where 9 is a power supply wiring and 11 is a ground wiring).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Applicant's admitted prior art (AAPA) as shown in instant figures 1A and B. Mori taught the device of claim 1 but did not expressly disclose the device further comprising four input pads being selectively connected. AAPA teaches in figure 1B four input pads 6 being selectively connected as instantly claimed.

Mori and AAPA are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to used the input pads as taught by AAPA in the device of Mori. The motivation for doing so is that the use of the pads would allow external connection to the internal circuitry of the device and thus allow proper device function. Therefore, it would have been obvious to combine Mori with AAPA to obtain the invention of claim 7.

Allowable Subject Matter

7. Claims 15 and 16 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action. Claims 9-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: the prior art teaches a capacitor, input/output and protection device formed under a pad region (see Mori for a capacitor, Sudo for a capacitor and input/output device and Fukuzumi et al for a protection device). However, the prior art did not teach the device further comprising second source voltage and ground wires, or the protection device comprising first and second wells formed in the substrate as instantly claimed.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional cited references teach structures generally considered relevant to applicant's field of endeavor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GEORGE C. ECKERT II
PATENT EXAMINER

GCE
May 23, 2002